**IN THE CLAIMS:**

Please cancel claims 12, 15, 18-19 and 25 without prejudice or disclaimer, and amend claims 1, 7, 13, 15 and 24 as follows:

1. (Currently Amended) A level conversion circuit comprising:

a first circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal for supplying a third signal having said second signal amplitude and being in a phase reverse to said first signal; and

a second circuit including a first p-channel type MOS transistor, a second p-channel type MOS transistor, a first n-channel type MOS transistor, a second n-channel type MOS transistor and, a third output terminal, a source of said first p-channel type MOS transistor being coupled to a first voltage terminal, a drain of said first p-channel type MOS transistor being coupled to a source of said second p-channel type MOS transistor, a drain of said second p-channel type MOS transistor and a drain of said first n-channel type MOS transistor being coupled to said third output terminal, a source of said first n-channel type MOS transistor being coupled to a drain of said second n-channel type MOS transistor and a source of said second n-channel type MOS transistor being coupled to a second voltage terminal,

wherein said second circuit is configured to form a fourth signal outputted from said third output terminal, said fourth signal having a signal level of said second signal amplitude and changing on the basis of the signal variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit whichever signal level changes faster to [[very]] vary a logical threshold of said second circuit so as to accelerate the variation of said fourth signal.

2. (Cancelled)

3. (Previously Presented) A level conversion circuit according to Claim 1, wherein a circuit from which, according to a signal inputted to the gate terminal of a MOS transistor, a signal matching said gate input signal is supplied to the source or drain

terminal of the MOS transistor is defined to be one stage, a number of MOS transistor stages gone via by a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said first output terminal is equal to a number of MOS transistor stages gone via by a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said second output terminal,

wherein a stage of said MOS transistor stages is defined as a gate-drain path or a gate-source path of a MOS transistor in the level conversion circuit.

4. (Original) A level conversion circuit according to Claim 1, wherein the state of said second p-channel type MOS transistor or first n-channel type MOS transistor in said second circuit varies with change in said second signal or third signal supplied from said first circuit.

5. (Previously presented) A level conversion circuit according to Claim 1, wherein a high resistance element for pull-up use and a high resistance element for pull-down use are connected respectively in parallel to said first p-channel type MOS transistor and said second n-channel type MOS transistor.

6. (Previously presented) A level conversion circuit according to Claim 1, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said first n-channel type MOS transistor.

7. (Currently Amended) A level conversion circuit according to Claim 1, wherein said first circuit comprises:

a first inverter for logically inverting said first signal;

a first node for receiving the output signal of said first inverter;

a third n-channel type MOS transistor;

a fourth n-channel type MOS transistor [[whose]] wherein the gate terminals of said third and fourth n-channel type MOS transistors are connected respectively to said first input terminal and said first node;

a third p-channel type MOS transistor whose source-drain path is connected in series to said third n-channel type MOS transistor and whose gate terminal is connected to the drain terminal of said fourth n-channel type MOS transistor; and

a fourth p-channel type MOS transistor whose source-drain path is connected in series to said fourth n-channel type MOS transistor and whose gate terminal is connected to the drain terminal of said third n-channel type MOS transistor, said first output terminal being connected to the drain terminal said fourth n-channel type MOS transistor, said second output terminal being connected to the drain terminal of said third n-channel type MOS transistor, and

wherein said second circuit comprises a second inverter for logically inverting said third signal being connected to said second output terminal.

8. (Previously Presented) A level conversion circuit according to Claim 7, wherein the state of said second p-channel type MOS transistor or first n-channel type MOS transistor in said second circuit varies with changes in said second signal or the output signal of said second inverter, whichever signal level changes faster.

9. (Previously Presented) A level conversion circuit according to Claim 8, wherein said second circuit further comprises a third inverter to control said first p-channel type MOS transistor and second n-channel type MOS transistor according to the second signal supplied from said first output terminal of said first circuit or the output signal of said second inverter, whichever is slower in signal variation.

10. (Cancelled)

11. (Original) A level conversion circuit, according to Claim 1, wherein the state of said first p-channel type MOS transistor or second n-channel type MOS transistor in said second circuit varies in response to a variation of said second signal or third signal supplied from said first circuit, whichever is faster.

12. (Cancelled)

13. (Currently Amended) A level conversion circuit ~~according to Claim 12~~, comprising:

a first circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal for supplying a third signal having said second signal amplitude and being in a phase reverse to said first signal; and

a second circuit configured to form a fourth signal outputted from a third output terminal, said fourth signal having a signal level of said second signal amplitude and changing on the basis of a variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit, whichever signal level changes faster to vary a logical threshold of said second circuit so as to accelerate the variation of said fourth signal,

wherein said second circuit has a first p-channel type MOS transistor, a second p-channel type MOS transistor, a first n-channel type MOS transistor and a second n-channel type MOS transistor whose source-drain paths are connected in series between a first voltage terminal and a second voltage terminal, the drain of said first p-channel type MOS transistor and the drain of said first n-channel type MOS transistor are connected to said third output terminal, high resistance elements are connected respectively in parallel to said second p-channel type MOS transistor and said [[first]] second n-channel type MOS transistor, and a delay means is provided to delay said second signal supplied from said first output terminal of said first circuit or said third signal supplied from said second output terminal of said first circuit to control said second p-channel type MOS transistor and first n-channel type MOS transistor or said first p-channel type MOS transistor and the second n-channel type MOS transistor.

14-15. (Cancelled)

16. (Previously Presented) A level conversion circuit according to Claim 1,

wherein said level conversion circuit is included in an input circuit or an output circuit of a semiconductor integrated circuit, and said input or output circuit is

connected to an external terminal at which signals of said second amplitude are supplied.

17. (Previously Presented) A level conversion circuit according to Claim 16, wherein said input or output circuit connected to said external terminal includes an inverse level conversion circuit for converting signals of said second amplitude into signals of said first amplitude.

18-19. (Cancelled)

20. (Reinstated) A level conversion circuit according to Claim 4, wherein a high resistance element for pull-up use and a high resistance element for pull-down use are connected respectively in parallel to said first p-channel type MOS transistor and said second n-channel type MOS transistor.

21. (Reinstated) A level conversion circuit according to Claim 5, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said first n-channel type MOS transistor.

22. (Reinstated) A level conversion circuit according to Claim 20, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said first n-channel type MOS transistor.

23. (Previously Presented) A level conversion circuit according to Claim 1, wherein the logical threshold of said second circuit is determined by relative gate widths or

24. (Currently Amended) A level conversion circuit according to Claim [[12]]13, wherein the logical threshold of said second circuit is determined by relative gate widths or relative gate width/gate length ratios of MOS transistors in said first and second circuits.

25. (Cancelled)